Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~——~~"), as is applicable:

1. (Currently amended) A method for verifying ~~core~~ determinacy of multiple cores of a single processor that operate in lockstep through testing of a modeled single processor, the method comprising:

extracting data stored in core model structures associated with modeled processor cores of the modeled single processor;

comparing the extracted data of one modeled processor core with extracted data of another modeled processor core to determine whether the modeled processor cores are operating in lockstep;

before core divergence occurs, determining if any mismatching data will cause core divergence; and

facilitating notice of an error if any mismatching data will cause core divergence.

2. (Original) The method of claim 1, wherein extracting data comprises extracting data from core data storage and interconnect elements.

3. (Original) The method of claim 2, wherein extracting data comprises extracting data from at least one of core buffers, core caches, core queues, core state variables, core state machines, and bus values.

4. (Original) The method of claim 1, wherein determining comprises accessing a data structure that matches divergence results with given mismatched data.

5. (Original) The method of claim 1, wherein determining comprises implementing an algorithm that uses the mismatched data as inputs.

6. (Currently amended) The method of claim 1, wherein facilitating notice comprises pending a check for a lockstep block checker to signal when divergence occurs, the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores.

7. (Original) The method of claim 6, wherein facilitating notice comprises flagging an error if the lockstep block checker does not signal that divergence occurred.

8. (Currently amended) The method of claim 1, further comprising first determining if a the modeled single processor is operating in lockstep mode.

9. (Currently amended) The method of claim 8, wherein determining if a the modeled single processor is operating in lockstep mode comprises analyzing at least one of a modeled lockstep block and a lockstep block checker, the modeled lockstep block being configured to monitor operation of the modeled processor cores and the lockstep block checker being configured to monitor operation of the modeled lockstep block.

10. (Currently amended) A system for verifying ~~core~~ determinacy of multiple cores of a single processor that operate in lockstep through testing of a modeled single processor, the system comprising:

means for determining if a the modeled single processor is operating in a lockstep mode;

means for extracting data stored in core model structures associated with modeled processor cores of the modeled single processor;

means for comparing the extracted data to determine if any data associated with one processor core does not match data associated with another processor core to determine whether the modeled processor cores are operating in lockstep; and

means for, before core divergence occurs, determining if any mismatching data will cause core divergence.

11. (Currently amended) The system of claim 10, wherein the means for determining if a the modeled processor is operating in a lockstep mode comprise means for analyzing at least one of a modeled lockstep block and a lockstep block

checker, the modeled lockstep block being configured to monitor operation of the modeled processor cores and the lockstep block checker being configured to monitor operation of the modeled lockstep block.

12. (Original) The system of claim 10, wherein the means for extracting data comprise means for extracting data from core data storage and interconnect elements.

13. (Original) The system of claim 10, wherein the means for determining if any mismatching data will cause core divergence comprise at least one of a data structure and an algorithm.

14. (Currently amended) The system of claim 10, further comprising means for pending a check for a lockstep block checker to signal when divergence occurs, the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores.

15. (Original) The system of claim 10, further comprising means for flagging an error.

16. (Currently amended) A ~~determinacy checker stored on a~~ computer-readable ~~medium~~ memory comprising a determinacy checker for verifying lockstep operation of multiple modeled cores of a modeled single processor, the ~~system~~ determinacy checker comprising:

logic configured to determine if a the modeled single processor is operating in a lockstep mode;

logic configured to extract data stored in core model structures associated with modeled processor cores of the modeled single processor;

logic configured to compare the extracted data to determine whether the modeled processor cores are operating in lockstep;

logic configured to determine if any data associated with one processor core does not match data associated with another processor core;

logic configured to determine if any mismatching data will cause core divergence before core divergence occurs; and

logic configured to facilitate notification of an error if any mismatching data will cause core divergence.

17. (Currently amended) The ~~checker~~ computer-readable memory of claim 16, wherein the logic configured to determine if a the modeled single processor is operating in a lockstep mode comprises logic configured to analyze at least one of a modeled lockstep block and a lockstep block checker, the modeled lockstep block being configured to monitor operation of the modeled processor cores and the lockstep block checker being configured to monitor operation of a modeled lockstep block.

18. (Currently amended) The ~~checker~~ computer-readable memory of claim 16, wherein the logic configured to extract data comprises logic configured to extract data from core data storage and interconnect elements.

19. (Currently amended) The ~~checker~~ computer-readable memory of claim 16, wherein the logic configured to determine if any mismatching data will cause core divergence comprises logic configured to access at least one of a data structure that matches divergence results with given mismatched data and an algorithm that uses the mismatched data as inputs.

20. (Currently amended) The ~~checker~~ computer-readable memory of claim 16, wherein the logic configured to facilitate notification comprises logic configured to pend a check for a lockstep block checker to signal when divergence occurs, the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores.

21. (Currently amended) The ~~checker~~ computer-readable memory of claim 16, wherein the logic configured to facilitate notification comprises logic configured to flag an error.

22. (Currently amended) A computer system, comprising:

a processing device; and

memory including a determinacy checker that verifies lockstep operation of multiple modeled cores of a modeled single processor, the determinacy checker being ~~is~~ configured to extract data stored in core model structures associated with modeled processor cores of the modeled single processor, compare the extracted data to determine whether the modeled processor cores are operating in lockstep, determine if any mismatching data will cause core divergence before core divergence occurs, and facilitate notification of an error if the mismatching data will cause core divergence.

23. (Original) The system of claim 22, wherein the checker is configured to extract data from core data storage and interconnect elements.

24. (Currently amended) The system of claim 22, wherein the checker is configured to pend a check for a lockstep block checker to signal when divergence occurs, the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores.

25. (Original) The system of claim 22, wherein the checker is configured to flag an error.